



Third-Generation AMD Opteron™ "Barcelona" Processor

AMD Japan
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AMD Quad-Core Processor Architecture A Closer Look at 'Barcelona'



Comprehensive
Upgrades
for SSE128

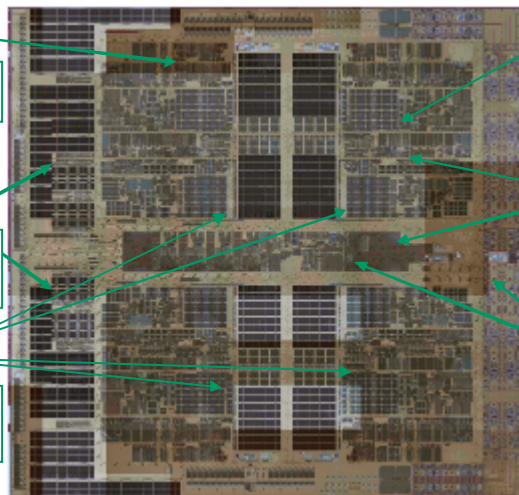
Can quadruple
floating-point
capabilities

New Highly Efficient
Cache Structure with
Shared L3 Cache

Balance of dedicated
and shared cache for
optimum quad-core
performance

CPU Core
Enhancements

To benefit applications by
improving overall efficiency
and performance of cores



Virtualization
Enhancements

New "Rapid Virtualization
Indexing" feature
designed for near native
performance on
virtualization applications

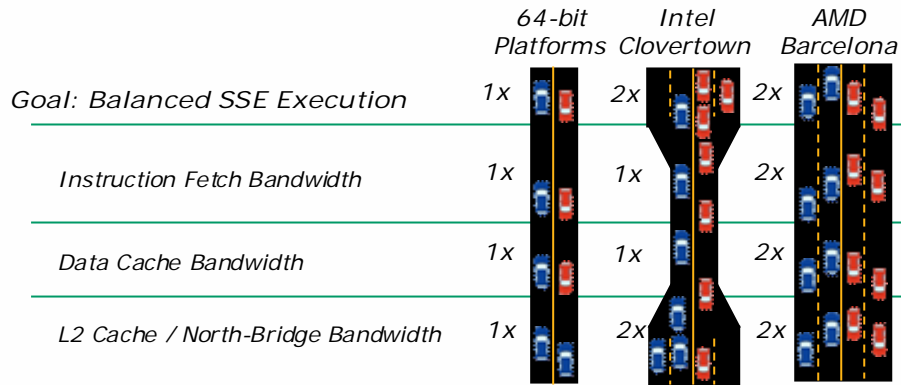
Advanced Power
Management

Provides granular
power management
resulting in improved
power efficiency

DRAM Controller
Enhancements

To improve overall
memory performance
with native
quad-core processing

'Barcelona' ... Not Just Four Cores Comprehensive 128-bit SSE Upgrades



- Barcelona doubles Instruction and Data pipelines ... Intel's pipeline doesn't
 - Helps keep 128-bit SSE pipeline full for optimum performance
- Dedicated 36-entry floating-point scheduler can reduce application latency
 - Intel 32-entry scheduler shared between floating-point and integer operations
- Incredible performance boost, per core, on target applications!

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Balanced, Highly Efficient Cache Structure



Dedicated L1

- AMD's 64KB/64KB (Data/Instruction) vs. Xeon's 32KB/32KB
- Allows 2 loads per cycle

Handle Data Quickly and Efficiently

Dedicated L2

- Dedicated cache designed to eliminate conflicts of shared cache structures
- Designed for true working data sets

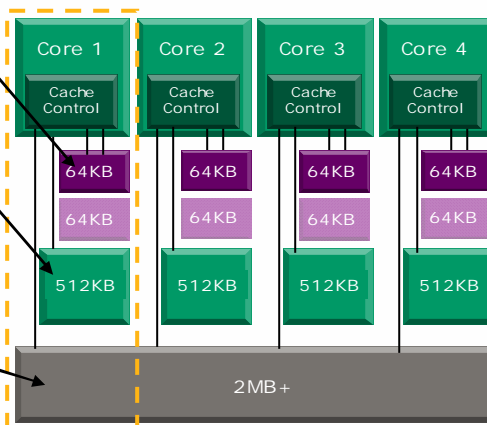
Avoid Thrashing
Minimize Latency

Shared L3 - NEW

- Designed for optimum memory use and allocation for multi-core
- Ready for expansion at the right time for customers

Reducing Latency to Main Memory

Efficient memory handling reduces need for "brute force" cache sizes



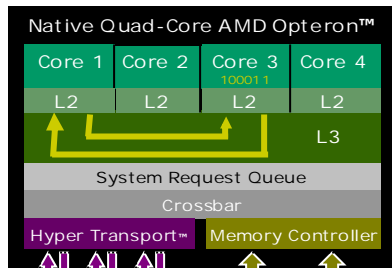
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Native Quad-Core Benefit: Faster Data Sharing



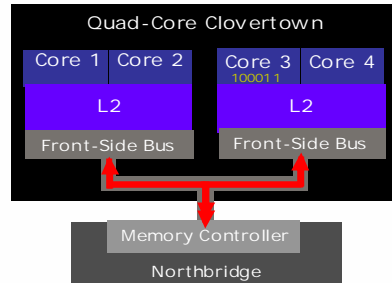
Situation: Core 1 needs data in Core 3's cache ... How Does it Get There?



1. Core 1 probes Core 3 cache, data is copied directly back to Core 1

This happens at processor frequency

**Result: Improved
Quad-Core Performance**



1. Core 1 sends a request to the memory controller, which probes Core 3 cache
2. Core 3 sends data back to the memory controller, which forwards it to Core 1

This happens at front-side bus frequency

**Result: Reduced
Quad-Core Performance**

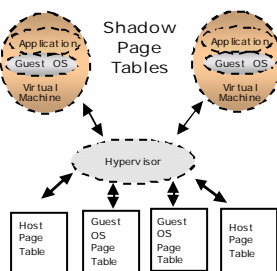
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AMD-V™ Enhancements: Rapid Virtualization Indexing Reduced Overhead for More Efficient Switching

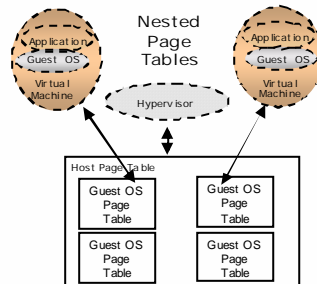


Dual Core



- Provides the guest OS with the illusion that it is managing its own world
- Page tables are actually kept up by the hypervisor in software
- Requires more software intervention from the hypervisor

Quad Core



- Each guest physically has their own world to manage
- Memory look ups done in hardware which can be faster than software management
- Requires less hypervisor intervention

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Better Power Savings With Dual Dynamic Power Management™

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Smarter Choices

Enables more AMD PowerNow!™ power saving opportunities

| Component Activity | | Associated <u>Core Voltage</u> and <u>Frequency</u> by Platform | | | | Example Workloads |
|--------------------|--------|---|----------|------------|----------|---|
| Cores | Memory | Unified | | DDPM | | |
| Busy | Busy | High Volts | High MHz | High Volts | High MHz | Virtualization, Multi-Tasking, Data analytics, Rendering, HPC |
| Idle | Idle | High Volts | Low MHz | Low Volts | Low MHz | Idle |
| Idle | Busy | High Volts | High MHz | Low Volts | Low MHz | DMA-based I/O (network traffic), web serving with a TOE, idle socket in a multi-socket system |

DDPM can offer 66% more power savings!

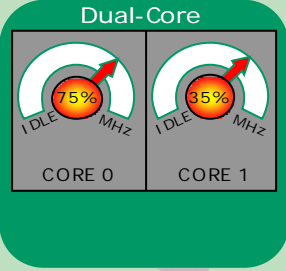
Many Workloads Benefit!

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Improving Processor Power Management with AMD PowerNow!™ Technology enhancements

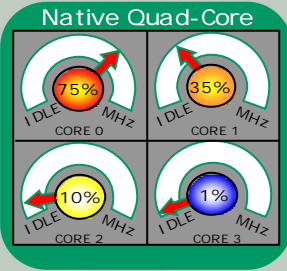
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Dual-Core



MHz and voltage is locked to highest utilized core's p-state

Native Quad-Core



MHz is independently adjusted separately per core. Voltage is locked to highest utilized core's p-state

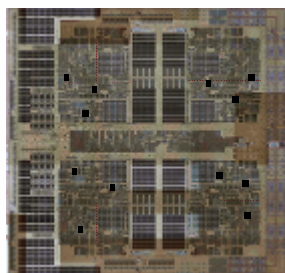
Native Quad-Core technology enables enhanced power management across all four cores

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Reducing Power with Advanced Logic Design



- Advanced logic design with additional clock gating
 - Hardware shuts down clock to areas of logic that are not used to reduce processor power consumption
 - Coarse Gaters
 - Shut down entire blocks of logic at a time
 - Fine Gaters
 - Shut down pieces of logic when appropriate



Reducing power consumption is a high priority in AMD processor designs

Example only: does not reflect actual areas of clock gating

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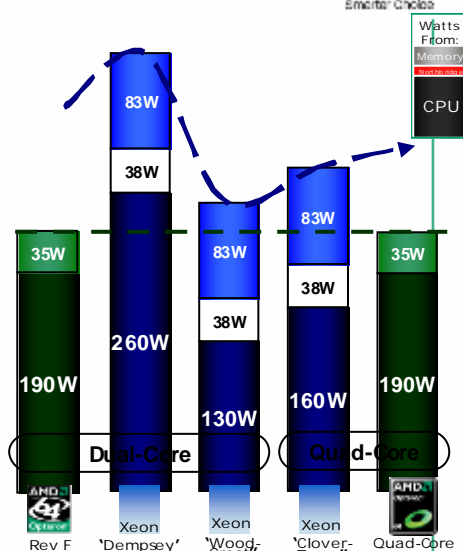
Seamless Quad-Core Power Migration Path

Reduces Operations cost



Consistent power & thermals makes it easier to:

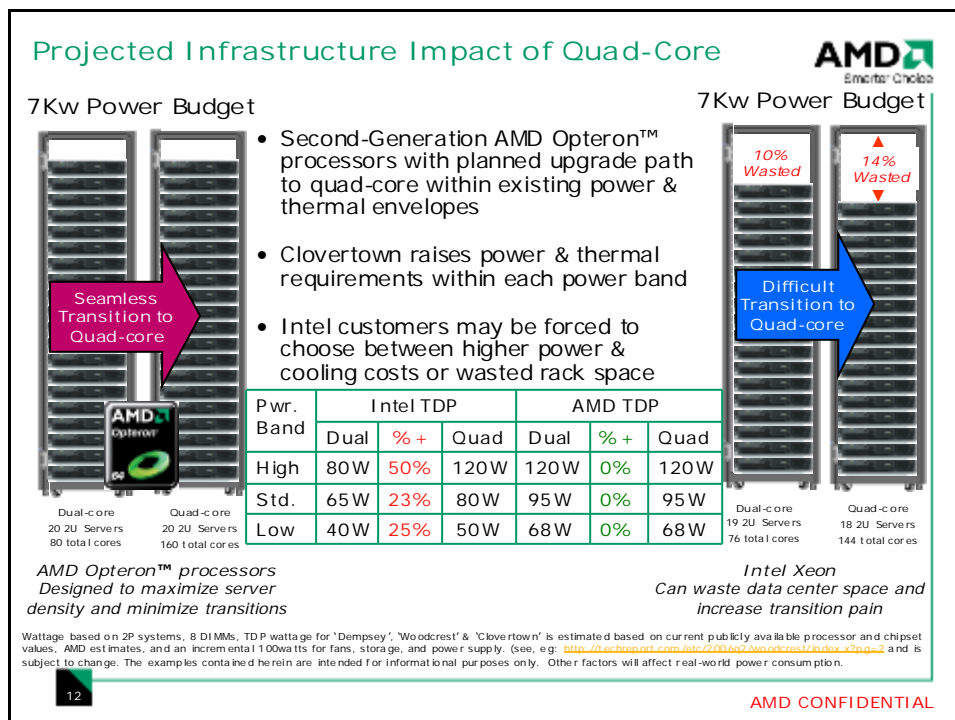
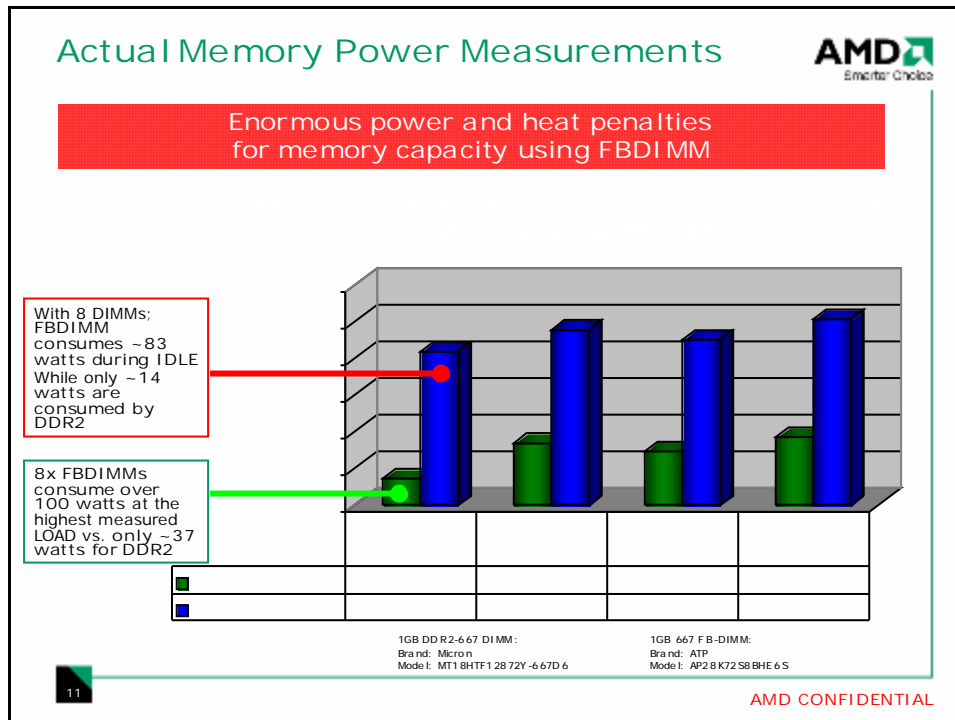
- Plan for long-term infrastructure needs
- Scale applications without increasing power consumption
- Upgrade to new systems without re-arranging racks
- Keep existing AC equipment instead of having costly upgrades



Wattage based on 2P systems with 8 DIMMs at max CPU wattage: Wattage for 'Dempsey', 'Woodcrest' and 'Clovertown' is estimated based on currently publicly available values (see, e.g.: <http://eeb.brown.com/eic/200602/woodcrest/index.x2p#2>) and is subject to change. The examples contained herein are intended for informational purposes only. Other factors will affect real-world power consumption.

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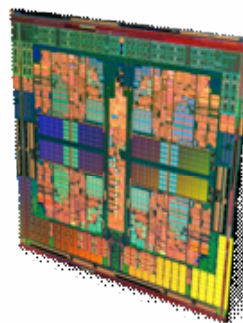


まとめ



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